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09/702,405	10/31/2000	David Hoyle	TI-30561	1217

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/702,405	HOYLE ET AL.
	Examiner	Art Unit
	David J. Huisman	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7,9-12 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,9-12 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 7, 9-12, and 14-19 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 8/18/2004.

Claim Objections

3. Claim 18 is objected to because of the following informalities: In line 3, replace "the second operand" with --the second source operand--. In line 4, replace "the first operand" with --the first source operand--. Appropriate correction is required.

4. Claim 19 is objected to because of the following informalities: In line 3, replace "the second operand" with --the second source operand--. In line 4, replace "the first operand" with --the first source operand--. Appropriate correction is required.

Withdrawn Rejections

5. Applicant, via amendments to the independent claims, has overcome the prior art rejections set forth in the final rejection. Consequently, the examiner has hereby withdrawn those rejections. However, upon further consideration, a new ground(s) of rejection is applied below.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-2, 7, 9, 12, and 14-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Abdallah et al., U.S. Patent No. 6,115,812 (as previously disclosed and herein referred to as Abdallah).

8. Referring to claim 1, Abdallah has taught a digital system comprising a microprocessor having an instruction execution pipeline with a plurality of pipeline phases (column 4, lines 32-35), wherein the microprocessor comprises:

a) program fetch circuitry operable to perform a first portion of the plurality of pipeline phases. It is inherent that some circuitry must exist in order to allow for the fetching of instructions. Instructions must be fetched in order to be executed. Looking at Fig. 1, program instructions are stored in memory 122 and they will be fetched into processor 110.

b) instruction decode circuitry connected to receive fetched instructions from the program fetch circuitry, the instruction decode circuitry operable to perform a second portion of the plurality of pipeline phases. See Fig. 1, component 116.

c) at least a first functional unit connected to receive control signals from the instruction decode circuitry, the functional unit operable to perform a third portion of the plurality of pipeline phases, the third portion being execution phases. See Fig. 1, component 112.

d) the functional unit comprising byte intermingling circuitry connected to receive a first source operand having a plurality of ordered fields and a second source operand having a plurality of ordered fields and having outputs connected to provide a destination operand in response to the control signals, wherein the byte intermingling circuitry is operable, responsive to one of a plurality of byte intermingling instructions, to place non-contiguous data from selected fields of the first source operand contiguously in a most significant portion of the destination operand, and to place non-contiguous data from selected fields of the second source operand that are at the same positions as the selected fields from the first source operand, contiguously in a least significant portion of the destination operand. See Fig.3D and column 6, line 25-42, and note the SHUFPS instruction. Note the first and second operands (340 and 342) are treated as four ordered fields each. In response to the instruction, any two of A, B, C, and D may be stored in any of the two high locations of the four-field destination while any two of E, F, G, and H may be stored in any of the two low locations of the four-field destination 346. As a result, it can be seen that non-contiguous A and D may be stored contiguously in the two high locations whereas non-contiguous E and H may be stored contiguously in the two low locations. This would result in the destination register holding A D E H.

9. Referring to claim 2, Abdallah has taught a system as described in claim 1. Abdallah, has further taught that the byte intermingling circuitry is operable to receive the first source operand and second source operand and to provide the destination operand during a single pipeline execution phase. See column 4, lines 32-35 and note that all of the packed instructions, which include SHUFPS (shuffle-pack), are completed within one clock cycle. Furthermore, a second way in which Abdallah reads on this claim is that each instruction is inherently either executed or

not executed. If an instruction is executed, then it goes through a single pipeline execution phase. Clearly, this is occurring in Fig.3D.

10. Referring to claim 7, Abdallah has taught a digital system comprising a microprocessor having an instruction execution pipeline with a plurality of pipeline phases (column 4, lines 32-35), wherein the microprocessor comprises:

a) program fetch circuitry operable to perform a first portion of the plurality of pipeline phases. It is inherent that some circuitry must exist in order to allow for the fetching of instructions. Instructions must be fetched in order to be executed. Looking at Fig.1, program instructions are stored in memory 122 and they will be fetched into processor 110.

b) instruction decode circuitry connected to receive fetched instructions from the program fetch circuitry, the instruction decode circuitry operable to perform a second portion of the plurality of pipeline phases. See Fig.1, component 116.

c) at least a first functional unit connected to receive control signals from the instruction decode circuitry, the functional unit operable to perform a third portion of the plurality of pipeline phases, the third portion being execution phases. See Fig.1, component 112.

d) the functional unit comprising byte intermingling circuitry connected to receive a first source operand having a plurality of ordered fields and a second source operand having a plurality of ordered fields and having outputs connected to provide a destination operand in response to the control signals, wherein the byte intermingling circuitry is operable, responsive to one of a plurality of byte intermingling instructions, to contiguously place the contents of a least significant plurality of contiguous fields selected from the second source operand in a least significant portion of the destination operand, and to contiguously place the contents of a most

significant plurality of contiguous fields from the first source operand in a most significant portion of the destination operand. See Fig.3D and column 6, line 25-42, and note the SHUFPS instruction. Note the first and second operands (340 and 342) are treated as four ordered fields each. In response to the instruction, any two of A, B, C, and D may be stored in any of the two high locations of the four-field destination while any two of E, F, G, and H may be stored in any of the two low locations of the four-field destination 346. As a result, it can be seen that least significant and contiguous G and H may be stored contiguously in the two low locations whereas most significant and contiguous A and B may be stored contiguously in the two high locations. This would result in the destination register holding A B G H.

11. Referring to claim 9, Abdallah has taught a digital system as described in claim 1. Abdallah has further taught a register file connected to the first functional unit for providing the first and second source operands and connected to the first functional unit to receive the destination operand. See Fig.1, component 114.

12. Referring to claim 12, Abdallah has taught a method of operating a digital system having a microprocessor and a set of byte intermingling instructions, comprising the steps of:

a) fetching a byte intermingling instruction for execution. It is inherent that some circuitry must exist in order to allow for the fetching of instructions. Instructions, such as the byte-intermingling SHUFPS instruction shown in Fig.3D, must be fetched in order to be executed. Looking at Fig.1, program instructions are stored in memory 122 and they will be fetched into processor 110.

b) fetching a first source operand and a second operand selected by the byte intermingling instruction, each of the first and second source operands comprising an ordered plurality of

fields. See Fig.3D and notice that two operands (340 and 342) must be fetched. Each of them is treated as four ordered fields.

c) writing, contiguously into a most significant portion of a destination operand, non-contiguous data from selected ones of the plurality of fields from the first source operand and writing, contiguously into a least significant portion of the destination operand, non-contiguous data from selected ones of the plurality fields from the second source operand that are at the same positions as the selected fields of the first source operand, the data being selected in accordance with the byte intermingling instruction. See Fig.3D and column 6, line 25-42, and note the SHUFPS instruction. In response to this instruction, any two of A, B, C, and D may be stored in any of the two high locations of the four-field destination while any two of E, F, G, and H may be stored in any of the two low locations of the four-field destination 346. As a result, it can be seen that non-contiguous A and C may be stored contiguously in the two high locations whereas non-contiguous E and G may be stored contiguously in the two low locations. This would result in the destination register holding A C E G.

13. Referring to claim 14, Abdallah has taught a method as described in claim 12. Abdallah has further taught that the step of writing is performed during a single execution phase of the microprocessor. See column 4, lines 32-35 and note that all of the packed instructions, which include SHUFPS (shuffle-pack), are completed within one clock cycle. Furthermore, a second way in which Abdallah reads on this claim is that each instruction is inherently either executed to provide a result or not executed. If an instruction is executed, then it goes through a single execution phase. Clearly, this is occurring in Fig.3D.

14. Referring to claim 15, Abdallah has taught a method as described in claim 12. Abdallah has further taught that the writing step contiguously writes most significant bytes of a plurality of fields selected from the second source operand into the least significant portion of the destination operand and contiguously writes most significant bytes of a plurality of fields selected from the first source operand into the most significant portion of the destination operand. Again, see Fig.3D, and note the SHUFPS instruction. In response to this instruction, any two of A, B, C, and D may be stored in any of the two high locations of the four-field destination while any two of E, F, G, and H may be stored in any of the two low locations of the four-field destination 346. As a result, it can be seen that most significant E and F (of the second operand) may be stored contiguously in the two low locations whereas most significant A and B (of the first operand) may be stored contiguously in the two high locations. This would result in the destination register holding A B E F.

15. Referring to claim 16, Abdallah has taught a method as described in claim 12. Abdallah has further taught that the writing step contiguously writes least significant bytes of a plurality of fields selected from the second source operand into the least significant portion of the destination operand and contiguously writes least significant bytes of a plurality of fields selected from the first source operand into the most significant portion of the destination operand. Again, see Fig.3D, and note the SHUFPS instruction. In response to this instruction, any two of A, B, C, and D may be stored in any of the two high locations of the four-field destination while any two of E, F, G, and H may be stored in any of the two low locations of the four-field destination 346. As a result, it can be seen that least significant G and H (of the second operand) may be stored contiguously in the two low locations of the destination whereas least significant C and D (of the

first operand) may be stored contiguously in the two high locations of the destination. This would result in the destination register holding C D G H.

16. Referring to claim 17, Abdallah has taught a method of operating a digital system having a microprocessor and a set of byte intermingling instructions, comprising the steps of:

a) fetching a byte intermingling instruction for execution. It is inherent that some circuitry must exist in order to allow for the fetching of instructions. Instructions, such as the byte-intermingling SHUFPS instruction shown in Fig.3D, must be fetched in order to be executed. Looking at Fig.1, program instructions are stored in memory 122 and they will be fetched into processor 110.

b) fetching a first source operand and a second operand selected by the byte intermingling instruction, each of the first and second source operands comprising an ordered plurality of fields. See Fig.3D and notice that two operands (340 and 342) must be fetched. Each of them is treated as four ordered fields.

c) contiguously writing, into a most significant portion of a destination operand, a most significant plurality of contiguous fields selected from the first source operand and contiguously writing, into a least significant portion of the destination operand, a least significant plurality of contiguous fields selected from the second source operand. See Fig.3D and column 6, line 25-42, and note the SHUFPS instruction. Note the first and second operands (340 and 342) are treated as four ordered fields each. In response to the instruction, any two of A, B, C, and D may be stored in any of the two high locations of the four-field destination while any two of E, F, G, and H may be stored in any of the two low locations of the four-field destination 346. As a result, it can be seen that most significant and contiguous A and B (of the first operand) may be

stored contiguously in the two high locations of the destination, whereas least significant and contiguous G and H (of the second operand) may be stored contiguously in the two low locations of the destination. This would result in the destination register holding A B G H.

17. Referring to claim 18, Abdallah has taught a digital system as described in claim 1. Abdallah has further taught that the byte intermingling circuitry is operable to contiguously place most significant bytes of a plurality of fields selected from the second operand into the least significant portion of the destination operand and to contiguously place most significant bytes of a plurality of fields selected from the first source operand into the most significant portion of the destination operand. Again, see Fig.3D, and note the SHUFPS instruction. In response to this instruction, any two of A, B, C, and D may be stored in any of the two high locations of the four-field destination while any two of E, F, G, and H may be stored in any of the two low locations of the four-field destination 346. As a result, it can be seen that most significant E and F (of the second operand) may be stored contiguously in the two low locations whereas most significant A and B (of the first operand) may be stored contiguously in the two high locations. This would result in the destination register holding A B E F.

18. Referring to claim 19, Abdallah has taught a digital system as described in claim 1. Abdallah has further taught that the byte intermingling circuitry is operable to contiguously place least significant bytes of a plurality of fields selected from the second operand into the least significant portion of the destination operand and to contiguously place least significant bytes of a plurality of fields selected from the first source operand into the most significant portion of the destination operand. Again, see Fig.3D, and note the SHUFPS instruction. In response to this instruction, any two of A, B, C, and D may be stored in any of the two high locations of the four-

field destination while any two of E, F, G, and H may be stored in any of the two low locations of the four-field destination 346. As a result, it can be seen that least significant G and H (of the second operand) may be stored contiguously in the two low locations of the destination whereas least significant C and D (of the first operand) may be stored contiguously in the two high locations of the destination. This would result in the destination register holding C D G H.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abdallah, as applied above, in view of Intel, IA-64 Application Developer's Architecture Guide, May 1999 (as applied in the previous Office Action and herein referred to as Intel).

21. Referring to claim 10, Abdallah has taught a digital system as described in claim 1. Abdallah has not taught that each of the set of byte intermingling instructions has a field for identifying a predicate register. However, Intel has taught instructions including fields for identifying predicates. See page 9-2 and more specifically the "qp" field in section 9.3.1. As is known in the art, and supported by Intel, predicates provide the user with more flexibility in that the user may decide if instructions should or should not be executed given a certain set of conditions. They also eliminate the need for an explicit conditional branch instruction because instructions become conditional based on the predicates. Consequently, to achieve increased

flexibility, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Abdallah to include fields for identifying predicates, as taught by Intel.

22. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abdallah, as applied above, in view of Haataja, U.S. Patent No. 6,137,836 (as applied in the previous Office Action).

23. Referring to claim 11, Abdallah has taught a digital system as described in claim 1. Abdallah has not taught that the digital system is a cellular telephone comprising the components set forth in claim 11. However, Haataja has taught a cellular telephone comprising:

a) an integrated keyboard connected to the CPU via a keyboard adapter. See Fig.8, component 72.

b) a display, connected to the CPU via a display adapter. See Fig.8, component 36.

c) radio frequency (RF) circuitry connected to the CPU. See Fig.8, component 56, and column 7, lines 6-11.

d) an aerial connected to the RF circuitry. See Fig.8, component 54.

It should be realized that Abdallah has taught a system that includes operations that increase the functionality and efficiency of the system. A person of ordinary skill in the art would have recognized that an improved processor (with more functionality) would lead to the overall improvement of the device in which it is embedded. As shown in Fig.8 of Haataja, and, as is well known in the art, cellular telephones are controlled by some sort of processor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have

the incorporate the digital system of Abdallah into a cell phone, as taught by Haataja, in order to improve the overall performance of the cell phone.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
September 30, 2004

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